Measurement Challenges for On-Wafer RF-SOC Test

Wai Yuen Lau
Senior Application Consultant
Agilent Technologies
1400 Fountaingrove Parkway, Santa Rosa, CA 95403

Brian Pugh
Director of Operations
Silicon Wave
6256 Greenwich Drive, Suite 300, San Diego, CA 92122

Abstract

With the wireless industry pushing towards higher levels of integration, employing more system-in-a-package (SIP) and multi-chip modules (MCM), known-good-die testing of RF-SOC devices has emerged as an important test challenge. These devices have higher packaging costs compared to the traditional single die integrated circuits (ICs), and potential lower yields, since multiple dice are used. As a result, the cost to perform comprehensive on-wafer testing is outweighed by the cost to scrap the devices during the final package test. In addition, some IC manufacturers are selling bare die to be used in the SIP or MCM of another manufacturer. On-wafer test is then required to ensure that good product is shipped.

This paper will use a Bluetooth radio modem chip as an example to discuss the measurement challenges and considerations for known-good die (KGD) testing of an RF-SOC device. With this example, the difficulty of testing RF functionality on-wafer will be compounded by the need to source and measure RF and digital signals simultaneously, creating signal integrity issues. This paper will explore the challenges of laying out the printed circuit board for the device under test (DUT), including setup of the wafer probe card and assembly. Factors taken into account when selecting a probe station, RF wafer probe card, and ATE test system will then be discussed. This paper will conclude with a discussion of on-wafer calibration, including challenges and solutions. Actual results from a Bluetooth radio modem chip will be used to further the discussion.

RF On-Wafer Measurement Challenges and Considerations

With the wireless semiconductor market moving towards higher levels of integration, the demand for KGD is creating many new challenges for wafer testing. This is especially true for today's chips that have both digital and RF functionality in them. Some of these on-wafer RF system on a chip (SOC) test measurement challenges and considerations are:

- Determining which tests are required to ensure a good die
- Selecting Automatic Test Equipment (ATE) and a wafer probe station that can meet these measurement requirements
- Determining the type of wafer probe assembly used to provide a clean test signal transition between the die and the ATE system
- Maintaining signal integrity on the probe card and device under test (DUT) board
- Understanding system calibration

Determining the Test Requirements for On-Wafer Test

There is always a tradeoff between quantity of testing, quality of testing, and testing costs. One must select a proper set of test parameters to ensure delivering a quality product while minimizing the cost of test. Examples of test parameters are: DC tests (such as continuity, sleep current, and operating current); digital logic verification (to ensure that all logic bits are functioning correctly); & purely RF measurements (such as power levels, harmonics, frequency settling time, noise figure (NF), and phase noise). There are other tests that require both digital and RF signals simultaneously; including most of a DUT receiver test suite.

The test measurement selections will influence which ATE you can use. For example, if the only test requirements are DC continuity and operating current, then the ATE system may only contain a DC power supply and a simple digital voltmeter (DVM). On the other hand, if the test requirements include DC continuity, operating current, digital logic control, RF power measurements, and Bit Error Rate (BER), then an ATE system that has DC power supplies, digital logic pin electronics, RF sources, AWG (if needed), RF measurement receiver, BER test receiver, and synchronization between the system digital and RF hardware is required.

As an example consider a Bluetooth radio modem IC. Such a device would likely require measurement of DC continuity, operating current, RF power levels, RF bandwidth, and Receive Sensitivity (based on BER) with and without interfering signals. One of the measurement challenges during the BER test is to have the RF and digital hardware working in unison. Timing and synchronization between the digital vector pattern to modulate the RF stimulus and the digitizer that receives the demodulated bit patterns from the DUT is critical. If the patterns do not synchronize and align correctly, a bad BER measurement can result. This alignment will vary depending on the hardware setup (such as cable length, and component delay). Having the capability to change the delay of the digital vector patterns in real-time will help ensure proper pattern alignment and timing synchronization. It is also important to have a single reference clock frequency to lock all the digital, analog, and RF hardware together to ensure proper synchronized timing.

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Selecting ATE and Probe Station

After determining which type of tests to perform on the chip, the next step is to determine which ATE test system best matches the requirements. As stated earlier, a test system can be as simple as a DVM and a DC power supply. But in most cases, a test system with more test capability will be required to provide the performance and accuracy demanded in this competitive market. In addition, to meet both current and future test requirements, one must select a tester that will allow expansion for future testing needs. As an example, a test system with RF, analog, digital, embedded memory, and scan is the ideal choice for the Bluetooth IC previously mentioned, as it will provide the necessary capability for the current designs and likely future enhancements. There are a variety of test system manufacturers today, including Agilent Technologies, Advantest, Teradyne, LTX, and Credence. Another important consideration when selecting a test system is the ability to interface with a wafer probe station and perform on-wafer RF-SOC test.

After choosing the ATE that meets the test requirements and supports on-wafer test, the wafer probe station must be selected. There are a variety of wafer probe station manufacturers today, including ElectroGlass and TSK. Some of the questions that should be considered during this selection phase are:

- What step size resolution is needed? This depends on the die spacing and the size of the pads being probed.
- What is the quality of the optical viewing? This feature is especially useful during alignment of the X, Y, and Z axes.
- Does the degree of wafer alignment and calibration meet the accuracy required of the alignment process? This is especially important for multi-site wafer probing because there are more probe points to align.
- Will wafer sorting, wafer mapping (see figure 1), and/or inking capabilities for post-production process be required to sort the good die from the bad die?
- Is the wafer probe station compatible with the test system selected?
- Can the ATE and the wafer probe station software function together?
- Is there shielding in the wafer probe station to create a low-noise environment for your measurements, such as when testing noise figure or low-level signals?
- Is temperature control required during wafer test?
- How fast can the probe card assembly be configured and reconfigured to the probe station? This is important as it will affect the up-time of your test cell.

After examining the different ATE and wafer probe stations available, a test solution would be chosen. The test solution found to meet all the requirements for the example device (Bluetooth radio modem IC) is shown in figure 2. The test system chosen provides all the necessary test capability, including:

- DUT power supplies
- Parametric measurement units (PMU)
- High-speed digital pin electronics
- Digital RF signal sources (with digital modulation capabilities)
- RF frequency hopping capability
- Three-tone RF stimulus capability
- RF measurement receivers
- BER test receivers

Figure 1. Wafer map plot (courtesy of TSK).

Figure 2. ATE used for on-wafer RF measurements (Agilent 93000 with RF Measurement Suite docked to a TSK wafer probe station).

Selecting the RF Wafer Probe Assembly

To provide a smooth signal transition between the die and the ATE measurement port, a proper RF wafer probe assembly must be selected. There are many probe manufacturers with different types of probe assemblies available. Some of the manufacturers are Cascade Microtech, GGB Industries, Inc., and SUSS MicroTec. Also, different types of probe assemblies are available, such as, needle probe, coplanar probe, Picoprobe®, and RFIC Pyramid™ probe. The test frequency range, port match, and number of test pins on the die are key elements that impact the selection of a wafer

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probe assembly. Each probe type has advantages and disadvantages. Needle probes, for example, are low cost, but are not designed for high frequencies. Coaxial probes have good port match, but other types of probes allow more pins. Some examples of the different types of probes can be seen in figures 3 and 4.

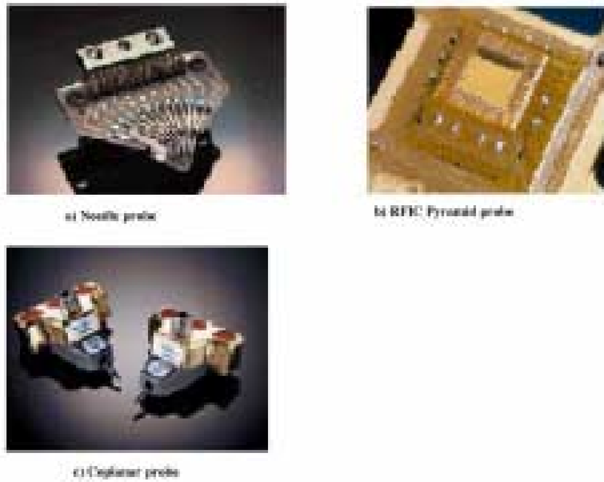

Figure 3. Different types of wafer probes (courtesy of Cascade Microtech)

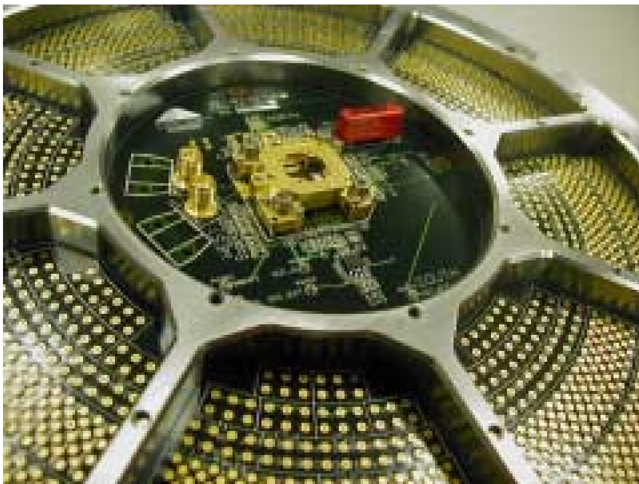

Figure 4. Example wafer probe card, shown with a RFIC Pyramid™ wafer probe core assembly (courtesy Silicon Wave and Cascade Microtech)

After identifying which type of probe to use, the next step is determining the probe footprint layout. What types of signal path structures are coming from the DUT? Is the signal path in the form of Ground-Signal (GS) layout, or is it in the form of Ground-Signal-Ground (GSG) layout? The wafer probe structure must match the die pattern layout. Each RF signal pad must have at least one adjacent RF ground for isolation in order to have good signal path design, and to provide a good RF launch between the die and probe. Many chip designers neglect to add extra grounds to each of the RF signal pads, and the results are poor RF measurements. For signal containment and ease of manufacturing, the coplanar (e.g., GSG) layout structure is the optimum choice. Having knowledge of RF design and signal integrity greatly improves the chances of meeting test requirements. Isolating the RF signals from other signal paths will improve the signal isolation and crosstalk. All grounds (RF, digital, and analog) must tie together at one point, as close to the chip as possible. This will help prevent ground loop problems. Communication between the chip designer and the test engineer is very important during the chip layout design phase.

Next, determine the pitch, or spacing between the pins, on the chip-probing pad. The wafer probe pitch needs to match the DUT pitch. If using coplanar probes, laying out the die-probing/bonding pattern to match the standard wafer probe pitch size from the probe manufacturer will reduce the wafer probe cost (e.g., no customization will be needed).

Planarity is an issue during setup and alignment of the probe tips to the wafer die. There are not many hardware component setups in the test system that allow adjustments for planarity Therefore, by selecting a probe that has some flexibility in the Z-axis movement will help improve the overall contact connections between the probe and the die. There are a number of other factors to consider:

- Probe and probe card impedance control is important to minimize reflections and interfering signals and also impact the repeatability of RF measurements.
- Having the ability to install decoupling capacitors on the probe core, or close to the DUT, will help reduce noise and oscillation problems.
- Being aware of how much current each probe trace needs to handle.
- Know what other supporting circuits are required in order for the DUT to operate correctly. If impedance-matching circuitry is required, then the matching network specification requirements must be provided to the probe manufacturer.

More signal integrity issues will be discussed in the next section. All of these issues must be considered before design and layout of the probe assembly. It is very important to work closely with your wafer probe manufacturer, and provide them the DUT interface requirements.

Maintaining Signal Integrity on the DUT Board and Probe Card

After deciding on the ATE and wafer probe assembly, the next step in the process is to consider the probe card and DUT board assembly. Figure 5 shows an overview of the wafer probe card hardware assembly setup. Signal integrity between the DUT and the ATE is important. The best designs will have a minimal amount of hardware components on the DUT board and probe card. The more components there are on these boards, the higher the possibility for problems to develop in the form of crosstalk, defective components, and mismatched transition. All of these problems will require time to troubleshoot.

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Ensure the DC power supply signals are clean by using filtering circuitry. Excess noise on the DC power supply lines may interfere with the operation of the DUT.

Figure 5. An overview of the wafer probe card hardware assembly setup. (courtesy of Agilent Technologies)

Having an easy docking interface between the probe assembly and the tester is important. On the production floor, a test cell may be used for many different devices; therefore, having a quick changeable interface will speed up the changeover and increase system utilization. One of the RF components that eases part changeover is the precision RF SMA type blindmate connectors in the testhead (see figure 6). These provide quick connect and disconnect of the DUT boards.

The impedance of the signal trace between the DUT and the wafer probe structure is the next consideration. It is important to get the proper trace interface between the DUT and the tester. Having the correct impedance will help to maximize the power transfer, and minimize reflections. Generally, for wireless devices, a RF port (trace) match of –14 dB or better will work. (Note: port match = [20*log(reflection coefficient)], and refers to how well the impedance of a port is matched to another structure. The lower the value, the better the port match. Trace inductance is another consideration during the layout phase. High inductance will cause discontinuity and degradation in performance. Differences in trace lengths also play important roles in determining if the DUT operation is correct. Different trace lengths can cause signal time delays, and delays between pins may cause improper DUT set-up.

Minimal crosstalk between traces is very important when making a low-level signal test. Therefore, it is important to separate the different signal traces enough or have a ground plane between them for isolation. As stated early, having RF design knowledge will help. For example, having enough via holes (spacing between via holes must be less than 1/10 of the highest operating frequency's wavelength) between the RF ground plane to reduce ground current noise and break up coupling energy is essential when measuring low level signals. Even better, place the different types of signals (e.g., DC, digital, and RF) on separate PC board layers. Keeping proper shielding and impedance on each signal line throughout the board assembly will also minimize crosstalk.

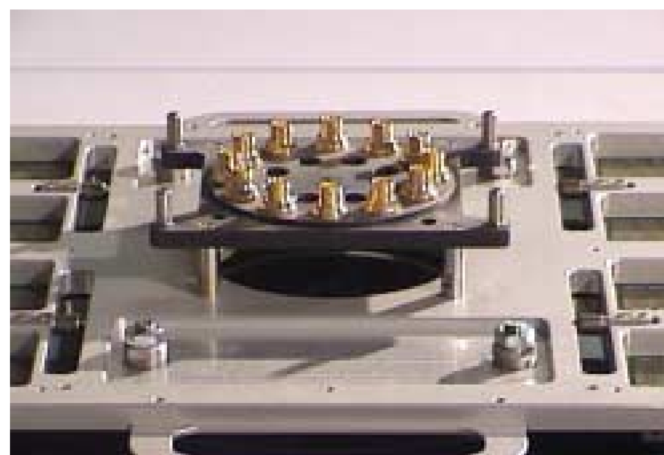

Figure 6. Precision RF blindmate connector assembly used for ease of docking (courtesy of Agilent Technologies)

RF Calibration

Typically, most digital test systems require digital hardware calibration every three to six months. However, for RF measurements, it is recommended that a RF calibration be performed whenever there's a change in temperature or hardware. If these parameters have changed from the last calibration, the RF measurement results will be less accurate and may affect the RF measurement results. Therefore, it is recommended t a RF calibration be done with each hardware setup, or once a week depending on the degree of measurement accuracy needed.

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There are a few different RF calibration options for wafer probing:

- Option 1: Calibrate with reference standards (e.g., Short, Open, and Load) at the tester RF ports, and then do an insertion loss offset of the wafer probe assembly.
- Option 2: Calibrate at the tester RF ports with reference standards, and then de-embed the wafer probe assembly using the probe's s-parameter data file (e.g., loss, phase, and match information). (See figure 7.)
- Option 3: Calibrate with "wafer reference standards" at the wafer probe tip.

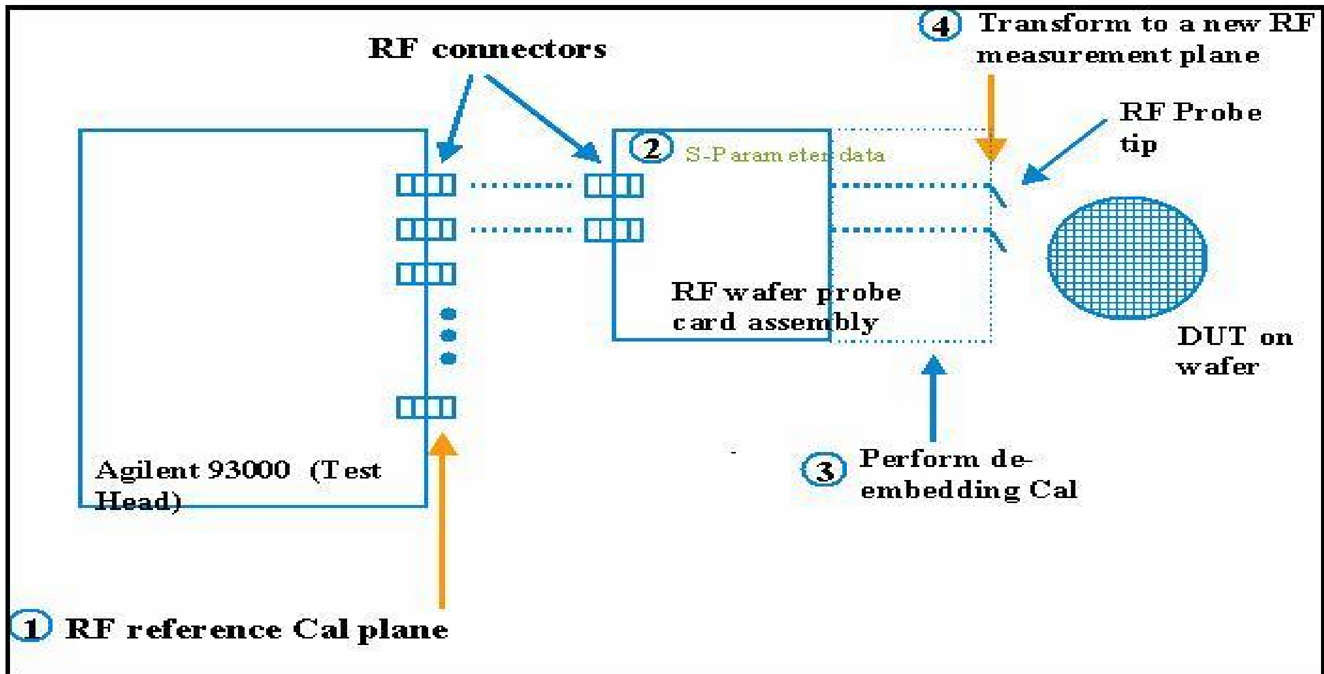

Figure 7. Overview of the RF calibration de-embedding process flow.

Each of the three options has advantages and disadvantages. The calibration choice depends on the measurement accuracy required, and the cost of setting up the calibration hardware. In production, if a measurement is repeatable and requires magnitude only (no phase information needed), then an offset correction factor will satisfy the measurement accuracy requirements. In that case, using Option 1 will be the appropriate calibration process. Option 3 is the most comprehensive calibration process. However, when developing a layout for the calibration standards, challenges may arise for a large integrated chip design (e.g., designing the standards to match the port layout positions.). It can also be time consuming during production calibration. In most cases, option 2 will give a sufficient level of calibration and accuracy. Option 2 is simple and requires minimum interaction from the user. The de-embedding file does not change unless the wafer probe card assembly hardware is changed. Most wafer probe manufacturers will supply this data file upon request. To produce the probe s-parameter data file, first perform a RF calibration using coaxial calibration standards at the ATE's RF ports. Then perform a second RF calibration at the probe tips using "wafer calibration standards". After calibration, perform normal two port s-parameter measurements on the probe assembly to get its performance data. This file will then be used for the de-embedded calibration process.

On-Wafer Test of the Bluetooth Radio Modem IC.

Now that the test system, probe station, and wafer probe assembly have been chosen (figure 8 shows a close-up of the on-wafer measurement hardware setup), it is time to discuss the test process development and measurement results.

Before starting the on-wafer RF measurement development, it is always a good idea to develop the test program with a packaged chip (DUT) form because a lot of complexity is added when a probe is put onto a wafer. This step will save time during the on-wafer development phase. For example, if any measurement problem does occur during on-wafer development, you will know the test program is not the cause.

Figure 8. A close-up of the on-wafer measurement hardware set up; shown with Agilent 93000 with RF Measurement Suite and TSK wafer probe station.

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Silicon Wave Case Study

The following plots are some of the on-wafer RF measurement results for the Silicon Wave SiW170X. The SiW170X, whose block diagram is shown in Figure 9, is a Bluetooth radio modem IC with three different interface options (SiW1701 with Silicon Wave Interface, SiW1702 with CDMA interface, and SiW1703 with GSM interface), available either in a plastic package or as a KGD. The SiW1702 KGD offers ~70% size reduction over packaged parts. The packaged and KGD versions of the SiW170X are both tested using the same test suite (shown in the table below).

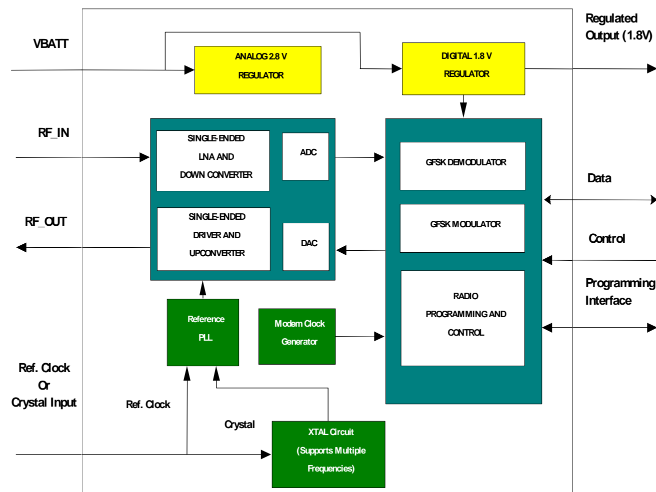

Figure 9. SiW170X Block Diagram

RF Transmit Tests	RF Receive Tests	DC/Digital Tests
Pout vs. Freq.	Receiver Sensitivity	Continuity
Pout vs. Gain Control	Max. Usable Signal	Leakage
Spurs	Co-channel Interference	Programming Interface Testing
Sideband Rejection	Adjacent Channel Interference	Regulator Voltages
Carrier Feedthrough	Out-of-Band blocking	Digital Modem Scan
Harmonic Distortion	IM2 & IM3	VCO lock Voltage
20-dB Bandwidth		TX/RX Active I
Synthesizer. Lock Time		Idle & Sleep I

SiW170X Test Suite Table

Figure 10 shows a Transmit (TX) mode CW output power plot at 2.402 GHz versus the DUT's output power gain control level ranges. For each gain control level, this device has approximately a 4 dB change. This test instructs the DUT to go into a TX mode, set the output frequency (or channel) and the gain level, and output a CW RF signal.

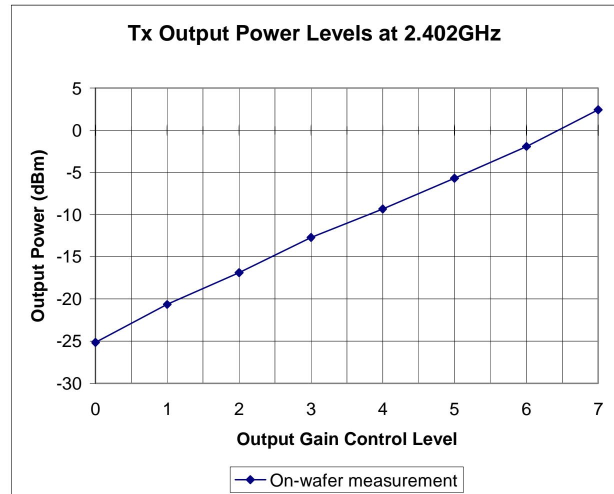

Figure 10. SiW170X RF power level versus output gain control setting

Figure 11 shows the same device tested at different output frequencies (channels) at a constant gain control setting. The measurement data show less than 1 dB of change over the tested frequency range. For a well designed IC, if the frequency response data shows a large deviation, the problem can often be tracked to an impedance mismatch between the probe card assembly and the DUT. Overall, these two measurement results show the TX output CW power of this device is operating within its specification limits.

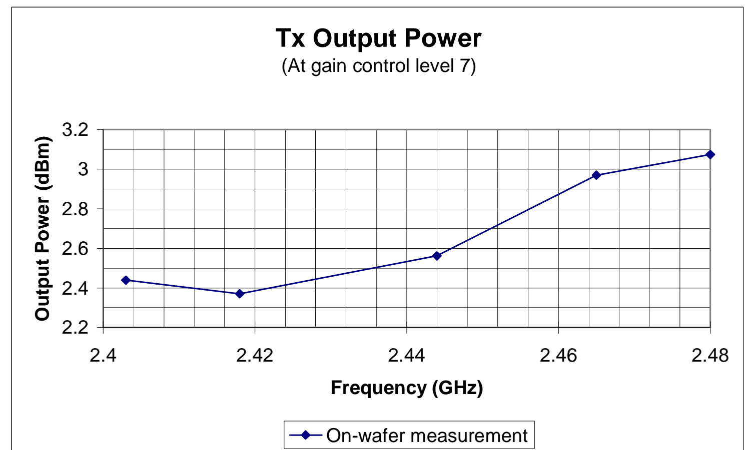

Figure 11. SiW170X RF power versus frequency

Figure 12 shows a modulated frequency response measurement plot of the DUT by using the "Time Domain" measurement feature of the tester. This test instructs the DUT to go to TX mode, with its output set to a modulated Bluetooth signal (2.441 GHz in this case). The tester

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measures this modulated RF signal on its RF port, down converts the RF signal to an IF signal, and digitizes the IF. The tester then outputs this data in the form of discrete "I" and "Q" data values. It performs an FFT on the "I" and "Q" data, calculates the amplitude and frequency step-size, and determines the 20dB-bandwidth points from the carrier's peak. The 20dB-bandwidth is the distance between the markers in this plot. The 20dB-bandwidth for this device is 856KHz, meeting the Bluetooth specification of less than 1 MHz.

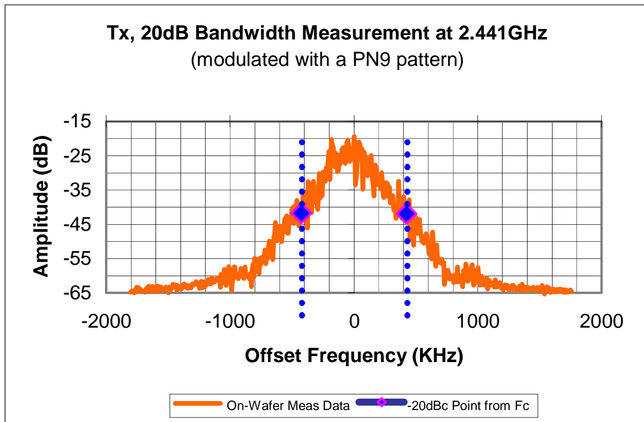

Figure 12. SiW170X Bandwidth measurement plot.

The receiver rf tests all measure BER under different stimulus conditions. The simplest of these is the receiver sensitivity test. In this measurement, the tester applies a PN9 modulated RF signal to the input port of the DUT and measures BER on its output pin. If the receiver meets the BER specification limit (0.1% for Bluetooth), then the tester will lower the input modulated RF power to the DUT, and repeat the test until the DUT exceeds the BER specification limit. The last input power level before the device fails the BER test will be the device's minimum receiver sensitivity value. In addition, BER tests are also performed in the presence of "interference tones." Those interference signals are strategically placed to interfere with and degrade the "desired" signal.

During the on-wafer development phase of the BER tests, one of the tester's key features was utilized extensively: the ability to change the data vector pattern in "real-time". The patterns used were "0000", "1111", "0101", and "PN9" to modulate the system RF stimulus. First, the DUT was tested with "0000" and "1111" modulation patterns, ensuring the die correctly captured all the bits. Next the "0101" data pattern was used for timing synchronization adjustment. Finally, the "PN9"data pattern was introduced to perform the actual BER test. Having this programming flexibility, with the digital and RF hardware working together, minimized test development time.

Conclusion

Making RF on-wafer measurements requires planning and coordination throughout the design and implementation phase. Understanding the test requirements and post-production processing requirements are key factors to consider before selecting the ATE and wafer probe station for on-wafer test of the target DUT.

After choosing the test system and probe station, the wafer probe assembly that meets the device requirements should be selected. Next, after taking into consideration issues such as signal grounding and signal impedance matching, the appropriate probe card and DUT board assembly can be designed to provide optimal signal integrity.

Once all of the hardware has been selected, designed, and assembled, the test system can be calibrated in order to provide accurate measurements.

As can be seen with the Bluetooth radio modem IC used in this study, a successful on-wafer test cell can be implemented if all of the important factors are taken into consideration.

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Agilent 93000 with RF Measurement Suite is a product of Agilent Technologies.

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RFIC Pyramid probe is a product of Cascade Microtech, Inc.

Picoprobe is a product of GGB Industries, Inc.

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